CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

at least one pad receiving at least one input signal;

a core; and

at least one input buffer circuit coupled between said pad and said core, said input buffer having a first mode where said input buffer circuit operates as an inverter, and a second mode wherein said input buffer circuit limits the voltage levels within the input buffer.

2. The integrated circuit of claim 9, wherein the first mode includes a normal mode where a supply voltage is applied to said input buffer circuit.

3. The integrated circuit of claim 9, wherein the second mode includes a live-insertion mode where a supply voltage is not applied to said input buffer circuit and an input signal is applied to said at least one pad.

4. An input buffer circuit having an input and a buffer output, said input buffer operable in a normal mode and a hot-plug mode, comprising:

a pull-up path coupled between a first circuit supply and the buffer output;

a pull-down path coupled between the buffer output and a ground reference voltage;

a first transistor coupled between the input and the pull-up path to activate the pull-up path;

a second transistor coupled between the input and the pull-down path to activate the pull-down path; and

a third transistor for protecting the pull-up path from over-voltage.

5. The input buffer circuit of claim 4, wherein the input buffer circuit is configured to prevent an over-voltage condition on each of the plurality of transistors and the input buffer circuit is configured to allow a hot-plug operation.

6. The input buffer circuit of claim 4, wherein the pull-up path includes:

a first reference voltage; and

a first pair of transistors including a first and second pull-up transistor coupled in series, said first pull-up transistor having a gate coupled with the first transistor and said gate biased by the third transistor and said second pull-up transistor having a gate biased by the first reference voltage.

7. The input buffer circuit of claim 6, wherein the pull-down path includes:

a second reference voltage; and

a second pair of transistors including a first and second pull-down transistor coupled in series, said first pull-down transistor having a gate coupled with the second transistor and said second pull-down transistor having a gate biased by the second reference voltage.

8. The input buffer circuit of claim 7, wherein the first reference voltage is approximately 1.0 volts, and the second reference voltage is approximately 2.5 volts.

9. The input buffer circuit of claim 4, further comprising:

a first bias voltage for biasing the first transistor; and

a second bias voltage for biasing the second transistor.

10. The input buffer circuit of claim 9, wherein the first bias voltage is approximately 1.0 volts during the normal mode and is approximately the input minus two diode drops during the hot-plug mode.

11. The input buffer circuit of claim 9, wherein the second bias voltage is approximately 2.5 volts during the normal mode and is approximately the input minus two diode drops during the hot-plug mode.

12. A method of operating an input buffer, comprising:

configuring the input buffer to operate substantially as an inverter in a normal mode; and

configuring the input buffer to operate substantially to limit internal voltage levels in a live insertion mode.